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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/721,566	11/22/2000	Jamal Ramdani	JG00060	2493

22850 7590 05/08/2003

OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C.
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EXAMINER

HU, SHOUXIANG

ART UNIT PAPER NUMBER

2811

DATE MAILED: 05/08/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/721,566

Applicant(s)

RAMDANI ET AL.

Examiner

Shouxiang Hu

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 18 March 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-28 is/are pending in the application.
- 4a) Of the above claim(s) 11-14 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☐ Claim(s) 1-10 and 15-28 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 5, 12, 14.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Claims 11-14 are withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected invention, there being no allowable generic or linking claim. Applicant timely traversed the restriction (election) requirement in Paper No. 16.

Applicant's election with traverse of Species I in Paper No. 16 is acknowledged. The traversal is on the ground(s) that the restriction requirement contains no basis for the distinctness of the restricted species. This is not found persuasive because, as stated in the previous Office action, Species I involves a template layer formed of surfactant layer and/or a Zintl layer; while Species II involves a template layer formed of a silicon layer and/or a SiC layer. Accordingly, Species I and Species II are patentably distinct as the material for the template in Species I is patentably substantially different from that of the template in Species II, and they are respectively suitable for the epitaxial growth of substantially different semiconductor materials, in view of the instant specification. According to MPEP § 809.02(a), should applicant traverse on the ground that the species are not patentably distinct, applicant should submit evidence or identify such evidence now of record showing the species to be obvious variants or clearly admit on the record that this is the case. However, applicant fails to provide or identify such evidence in the arguments.

The requirement is still deemed proper.

Claim Objections

2. Claims 9, 18 and 23-27 (as originally presented) are objected to because of the following informalities and/or defects:

Among the originally presented claims, there are two claims both numbered as claim 23. In this office action, the misnumbered claims, from the second claim 23 through claim 27 (the original ones) have been hereafter renumbered as claims 24-28, respectively.

In addition, claims 9, 18 and 27 (renumbered one) recite the terms of "the cap inducing material", "the monocrystalline Group IV substrate" and "the amorphous oxide layer", respectively, but there is insufficient antecedent basis for any of the terms in these claims.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-10, 15-20 and 23-28 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential elements, such omission amounting to a gap between the elements. See MPEP § 2172.01. The omitted elements are: an amorphous silicon oxide layer formed between the substrate and a perovskite oxide buffer. It is not clear how the lattice mismatch in the instant invention can be solved without such an amorphous silicon oxide layer.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 2, 5-9, 23-25 and 28 (renumbered ones), insofar as being in compliance with 35 U.S.C. 112, are rejected under 35 U.S.C. 102(b) as being anticipated by Kao et al. ("Kao"; US 5,391,515; of record).

First, it is noted again that the originally misnumbered claims, from the second claim 23 through claim 27, have been respectively renumbered as claims 24-28 in this office action.

Kao discloses a semiconductor structure (Figs. 3a-3d), comprising: a monocrystalline substrate (102; Si); a buffer layer (104); a template (106 and 108); and a monocrystalline material (110; GaAs).

Regarding claim 2, it is noted that the template layer of AIAs (108) in Kao is readable as a Zintl type phase material.

Regarding claims 5-9, it is noted that at least the bottom portion of the template layer of AlGaAs (106) in Kao is readable as a surfactant material comprising Al; and the template layer of AIAs (108) is readable as a capping layer comprising As. And, it is further noted that the limitation of "formed by exposing the surfactant material to a cap inducing material" recited in claim 8 does not carry patentable weight in the claims

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drawing to a structure, because distinct structure is not necessarily produced. In re Thorpe, 227 USPQ 964, 966 (Fed. Cir. 1985).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 15-16, 26 and 27, insofar as being in compliance with 35 U.S.C. 112, are rejected under 35 U.S.C. 103(a) as being unpatentable over Kao et al. ("Kao"; US 5,391,515; of record) in view of Galviello et al. ("Galviello"; US 5,356,831; of record).

The disclosure of Kao is discussed as applied to claims 1, 2, 5-9, 23-25 and 28 above.

Kao further teaches to form an amorphous silicon oxide layer between the substrate and the buffer layer (see col. 6, lines 48-52).

Although Kao does not expressly disclose that the buffer layer can also be formed of monocrystalline oxide such as SrTiO_3 , one of ordinary skill in the art would readily recognize that SrTiO_3 is an art-recognized buffer layer for the epitaxial growth of GaAs with good quality, as evidenced in Galviello (see col. 2, lines 54-68).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the SrTiO_3 buffer layer of Galviello into the

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semiconductor structure of Kao, so that a semiconductor structure with good quality in the epitaxially grown GaAs layer would be obtained.

Regarding claims 26 and 27, it is noted that the thickness of the buffer layer and the thickness of the amorphous silicon oxide layer are both art-recognized parameters of importance subject to routine experimentation and optimization; and that a buffer layer thickness of 5 nm is well within the commonly recognized thickness range for a buffer layer in the art (as evidenced in Pessa et al.; US 4,876,218; see col. 2, lines 43-47, and, col. 4, lines 5-7). Therefore, it would be well within the ordinary skill in the art to form the semiconductor structure collectively taught above by Kao and Galviello with the thickness of the buffer layer and amorphous oxide layer being respectively 2-10 nm and 5-6 nm, so that a semiconductor structure with optimized epitaxial growth and/or performance would be obtained.

7. Claims 17-22, insofar as being in compliance with 35 U.S.C. 112, are rejected under 35 U.S.C. 103(a) as being unpatentable over Kao in view of galviello, as applied to claims 15-16, 26 and 27 above, and further in view of Bisaro et al. ("Bisaro"; US 5,141,894; of record).

The disclosures of Kao and galviello are discussed as applied to claims 15-16, 26 and 27 above.

Although Kao and Galviello do not expressly disclose that the monocrystalline SrTiO_3 buffer layer can be converted to an amorphous oxide buffer layer, one of ordinary skill in the art would readily recognize that the conversion of a buffer layer to an

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amorphous buffer layer is desirable for reducing the dislocations in the epitaxially grown GaAs layer, as evidenced Bisaro (see the conversion of the buffer layer 16 to an amorphous buffer layer 15 in Fig. 4d; also see col. 4, line 64, through col. 5, line 11).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to make the above semiconductor structure collectively taught by Kao and galviello with the buffer oxide layer being converted to an amorphous buffer layer, as taught in Bisaro, so that a semiconductor structure with reduced dislocations in the epitaxially grown GaAs layer would be obtained.

Regarding claims 18-20, all of the limitations regarding the lattice features and the orientation features recited in these claims would be naturally met in the above collectively taught semiconductor structure, as it would have been formed of a structure and a material set both substantially the same as that of the instant invention.

Double Patenting

8. A rejection based on double patenting of the "same invention" type finds its support in the language of 35 U.S.C. 101 which states that "whoever invents or discovers any new and useful process ... may obtain a patent therefor ..." (Emphasis added). Thus, the term "same invention," in this context, means an invention drawn to identical subject matter. See *Miller v. Eagle Mfg. Co.*, 151 U.S. 186 (1894); *In re Ockert*, 245 F.2d 467, 114 USPQ 330 (CCPA 1957); and *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970).

1.

A statutory type (35 U.S.C. 101) double patenting rejection can be overcome by canceling or amending the conflicting claims so they are no longer coextensive in scope. **The filing of a terminal disclaimer cannot overcome a double patenting rejection based upon 35 U.S.C. 101.**

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9. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b)

2. 37 CFR 1.78(b) provides that when two or more applications filed by the same applicant contain conflicting claims, elimination of such claims from all but one application may be required in the absence of good and sufficient reason for their retention during pendency in more than one application.

3.

10. Double-patenting conflicts exist between claims of the following related issued patents and co-pending applications which includes the present application.

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09273929	09755691	09882063	09906138	09911445	09921905	10017596
09274268	09758723	09882064	09906730	09911446	09921910	10020898
09425945	09766046	09882067	09906769	09911447	09924481	10020900
09465623	09780119	09884082	09906782	09911448	09927393	10026446
09584601	09795784	09884149	09906783	09911455	09927396	10026812
09607207	09801881	09884150	09906784	09911456	09928356	10053588
09607236	09813779	09884981	09907703	09911457	09929018	10059409
09607237	09822499	09884982	09907704	09911458	09929019	10059411
09607239	09822499	09884983	09907705	09911459	09929020	10062429
09607386	09824259	09885409	09907707	09911460	09929021	10076450
09607408	09824273	09897059	09908695	09911464	09929022	10091452
09607420	09824376	09897128	09908707	09911465	09929024	10124460
09607434	09824388	09897965	09908860	09911466	09929261	10125410
09607722	09824615	09897968	09908883	09911469	09929748	10125486
09607744	09832354	09899996	09908885	09911472	09930145	10125540
09608807	09838273	09899997	09908886	09911473	09930170	10128262
09609071	09840213	09900882	09908887	09911475	09930171	10134506
09609262	09842734	09900883	09908888	09911478	09930175	10136324
09617640	09842735	09900885	09908891	09911484	09930176	10137369
09621130	09849159	09900887	09908892	09911487	09930188	10137383
09621771	09849172	09900921	09908897	09911488	09930243	10140939
09621779	09852109	09901109	09908898	09911490	09930247	10141876
09624296	09853744	09901110	09908902	09911491	09930254	10145734
09624526	09859700	09901601	09909905	09911492	09930259	10150065
09624690	09861636	09901905	09909906	09911493	09930260	10150066
09624691	09861637	09903740	09909936	09911494	09930261	10151950
09624698	09861638	09903741	09909937	09911495	09930270	10152783
09624699	09861639	09903742	09909938	09911496	09930275	10161743
09624754	09865428	09903743	09909939	09911496	09930276	10166196
09624803	09865429	09903784	09909940	09911507	09930278	
09624877	09865446	09904841	09909941	09911517	09930308	
09625100	09865447	09904892	09910018	09911518	09930444	
09629283	09865448	09904894	09910019	09911539	09934836	
09642558	09865449	09904895	09910020	09911542	09960402	
09656337	09866637	09905098	09910021	09911543	09975930	
09662390	09870589	09905110	09910022	09911627	09978096	
09669602	09870592	09905115	09910023	09911628	09983326	
09678372	09870828	09905116	09910024	09911629	09983854	
09689583	09870829	09905863	09910032	09911691	09983859	
09692568	09870830	09905868	09910034	09911702	09983866	
09712425	09870831	09905869	09910035	09918801	09983869	
09712875	09870832	09905902	09910044	09918802	09984471	
09721566	09870833	09905903	09910753	09919927	09985757	
09733181	09870834	09905930	09910754	09919967	09986024	
09733688	09870835	09905932	09910798	09921894	09986034	
09740219	09870836	09905933	09910799	09921895	09986534	
09740268	09870837	09905934	09911412	09921896	09986899	
09753808	09871958	09905935	09911420	09921898	09993514	
09755340	09874984	09905980	09911429	09921900	09993523	
09755341	09882062	09905981	09911444	09921901	09994066	

Serial Numbers of Related Issued Patents and Co-pending Applications (shown above)

11. While it is true that the Examiner has the burden to show how a rejection is specifically applied to each claim, the exemplary showing with respect to the claims individually discussed below establishes a *prima facie* showing of the unpatentability of the instant claims and is sufficient to give the applicant fair notice of how the rejection is applied to each and every other claim. Further, an analysis of all of the claims in the approximately 330 related applications would be an extreme burden on the Office requiring millions of claim comparisons. Accordingly, the Office is shifting the burden to the applicants to show, if they can, patentable distinctions between the instant claims and those of the other applications and patents. Specifically, in order to resolve the conflict between applications, applicant is required to:

- (1) file terminal disclaimers in each of the related applications terminally disclaiming each of the other approximately 330 applications;
- (2) provide a statement attesting to the fact that all claims in the approximately 330 applications have been reviewed by applicant and that no conflicting claims exists between the applications. Applicant should provide all relevant factual information including the specific steps taken to insure that no conflicting claims exist between the applications; or;
- (3) resolve all conflicts between the claims in the above identified approximately 330 applications by identifying how all the claims in the instant application are distinct and separate inventions from all of the claims in all of the other approximately

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330 identified applications. Note: the examples provided below are merely illustrative of the overall problem. Only addressing/correcting the specifically identified conflicts would **not** satisfy the requirement.

Further, due to Applicant's better familiarity with the related applications, Applicant now has the burden of confirming that the preceding list is accurate and complete, or must take appropriate action(s) to assure that no such conflicts exist in any other applications that have been inadvertently omitted from the preceding list, but do in fact possess related subject matter.

Applicant is reminded that obviousness-type double patenting analysis entails a two-step process: (1) the claims of this application and the other approximately 330 applications must be construed; and (2) the claims of this application must be compared with the claims of the other applications to determine whether the differences in subject matter between the two claims render the claims patentably distinct. See Georgia-Pacific Corp. v. United States Gypsum Co., 195 F.3d 1322, 1326, 52 USPQ2d 1590, 1593 (Fed. Cir. 1999), and General Foods Corp. v. Studiengesellschaft Kohle, 972 F.2d 1272, 1279, 23 USPQ2d 1839, 1844 (Fed. Cir. 1992). As the Court of Customs and Patent Appeals (CCPA) explained: "[t]he fundamental reason for the rule [against "double patenting"] is *to prevent unjustified timewise extension of the right to exclude* granted by a patent no matter how the extension is brought about." In re Van Ornum, 686 F.2d 937, 943-44, 214 USPQ 761, 766 (CCPA 1982) (brackets and emphasis in the original) (quoting In re Schneller, 397 F.2d 350, 354, 158 USPQ 210, 214 (CCPA 1968)).

Failure to comply with the above requirement will result in abandonment of the application. However, the requirement will be held in abeyance until allowable subject matter has been indicated by the examiner.

12. The following claim comparisons are examples of conflicts between three of the copending applications:

S.N. 09/908,892; claims 11

A process for fabricating a semiconductor structure comprising:

- providing a monocrystalline silicon substrate;
- depositing a monocrystalline perovskite oxide film overlying the monocrystalline silicon substrate, the film having a thickness less than a thickness of the material that would result in strain-induced defects;
- forming an amorphous oxide interface layer containing at least silicon and oxygen at an interface between the monocrystalline perovskite oxide film and the monocrystalline silicon substrate;
- epitaxially forming a layer of intermetallic compound overlaying the monocrystalline perovskite oxide film; and
- epitaxially forming a monocrystalline compound semiconductor layer overlying the layer of intermetallic compound.

S.N. 09/755,340; claims 17, 19 and 20:

[Claim 17] A process for fabricating a semiconductor structure comprising the steps of:

- providing a monocrystalline substrate;
 - epitaxially growing [an] accommodating buffer layer overlying the monocrystalline substrate;
 - forming an amorphous layer on the monocrystalline substrate during the growth of the accommodating buffer layer; and
 - forming a monocrystalline conductive layer over the accommodating buffer layer;
- [Claim 19] epitaxially growing an additional monocrystalline layer above the monocrystalline conductive layer;
- [Claim 20] wherein the step of [claim 19] includes growing a semiconductor material layer.

S.N. 09/986,024; claim 169:

A process for fabricating a semiconductor structure comprising:

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providing a monocrystalline silicon substrate;
depositing a monocrystalline perovskite oxide film overlying the monocrystalline silicon substrate, the film having a thickness less than a thickness of the material that would result in strain-induced defects;
forming an amorphous oxide interface layer containing at least silicon and oxygen at an interface between the monocrystalline perovskite oxide film and the monocrystalline silicon substrate; and
epitaxially forming a monocrystalline compound semiconductor layer overlying the monocrystalline perovskite oxide film.

4. A comparison of the claims shows that all three applications set forth the method steps of providing a monocrystalline substrate; an accommodating buffer (or perovskite) layer; an amorphous oxide interface therebetween; and at least a monocrystalline semiconductor layer over the buffer/perovskite. The respective sets of claims are not identical because:

5. Claims 17, 19 and 20 of the '340 application are broader than claim 11 of the '892 application because the '340 claims do not further require that the monocrystalline substrate be Si; that the amorphous oxide interface layer also contain silicon; that the accommodating buffer specifically be a monocrystalline perovskite; that the conductive layer specifically be an intermetallic compound; nor that the monocrystalline semiconductor layer be a compound monocrystalline semiconductor layer.

6. Claim 169 of the '024 application is broader than claim 11 of the '892 application because the '024 claim does not require the additional presence of the epitaxially grown intermetallic compound layer.

7. Accordingly, claims 17, 19 and 20 of the '340 application are rejected under the judicially created doctrine of obviousness-type double patenting as being

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unpatentable over claim 11 of the copending '892 application. Although the conflicting claims are not identical, they are not patentably distinct from each other because claim 11 of the '892 application anticipates claims 17, 19 and 20 of the '340 application as explained above. See e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985) for the proposition that an obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but an examined application claim is not patentably distinct from the reference claim(s) because the examined claim is either anticipated by, or would have been obvious over, the reference claim(s). This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

8. Similarly, claim 169 of the '024 application is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 11 of the copending '892 application. Although the conflicting claims are not identical, they are not patentably distinct from each other because claim 11 of the '892 application anticipates claim 169 of the '024 application as explained above. This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

13. While not specifically addressed herein, similar double-patenting conflicts also exist between the product claims of various applications as well. Moreover, while the Office has a long established policy of generally requiring restrictions between semiconductor product claims (class 257) and method claims (class 438) in a given

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application, this policy does not negate Applicant's responsibility for ensuring that no conflicts exist between those applications presenting product claims and those applications presenting method claims. This is because it is also well established agency policy that restricted product and method claims may be subject to rejoinder during the course of prosecution. See MPEP 821.04.

Allowable Subject Matter

14. Claims 3, 4 and 10 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, and the double patenting rejection, both set forth in this Office action.

Reasons for Allowance

15. The following is an examiner's statement of reasons for allowance: Prior art does not teach or render obvious a semiconductor structure as defined in claims 3, 4 and 10, comprising particularly: a template formed of a specifically defined Zintl type phase material as the one recited in claims 3 and 4, or a template formed of a surfactant comprising Al and a capping layer comprising Al_2Sr for the epitaxial growth of GaAs, wherein the template is formed on a buffer layer comprising a perovskite oxide layer overlying an amorphous silicon oxide layer.

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Conclusion


16. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Reference A is cited as being related to a GaAs-on-Si substrate.

17. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shouxiang Hu whose telephone number is (703) 306-5729. The examiner can normally be reached on Monday through Thursday, 7:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (703) 308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9318 for regular communications and (703) 872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

SH
May 5, 2003


Shouxiang Hu
Patent Examiner
TC2800